sparc v8 instruction set

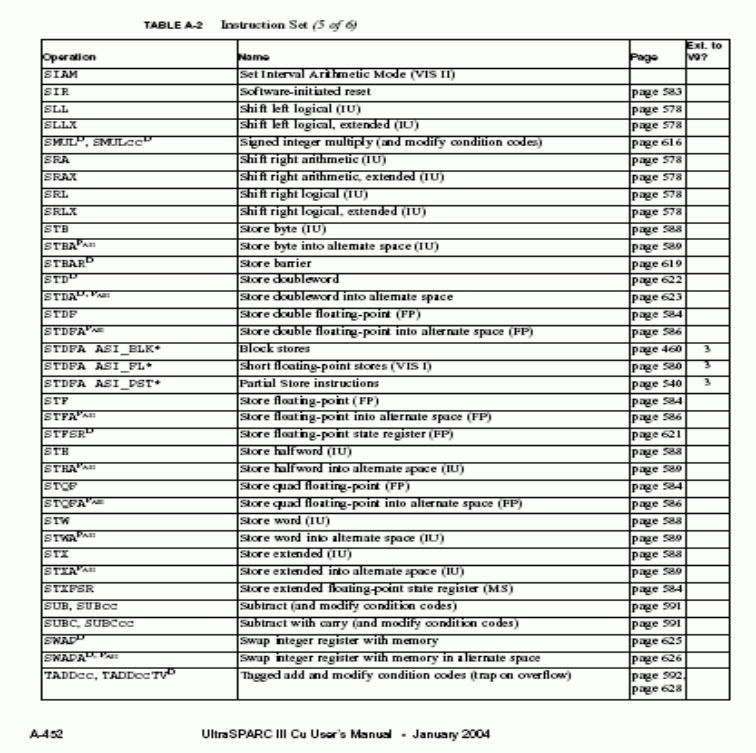

TABLE A-2 Instruction Set (5 of 6)

Operation	Name	Page	Ext. to V9?
SIAM	Set Interval Arithmetic Mode (VIS II)		
SIR	Software-initiated reset	page 583	
SLL	Shift left logical (IU)	page 578	
SLLX	Shift left logical, extended (IU)	page 578	
SMUL[D], SMULcc[D]	Signed integer multiply (and modify condition codes)	page 616	
SRA	Shift right arithmetic (IU)	page 578	
SRAX	Shift right arithmetic, extended (IU)	page 578	
SRL	Shift right logical (IU)	page 578	
SRLX	Shift right logical, extended (IU)	page 578	
STB	Store byte (IU)	page 588	
STBA[P_AS]	Store byte into alternate space (IU)	page 589	
STBAR[D]	Store barrier	page 619	
STD[D]	Store doubleword	page 622	
STDA[D, P_AS]	Store doubleword into alternate space	page 623	
STDF	Store double floating-point (FP)	page 584	
STDFA[P_AS]	Store double floating-point into alternate space (FP)	page 586	
STDFA ASI_BLK*	Block stores	page 460	3
STDFA ASI_PL*	Short floating-point stores (VIS I)	page 580	3
STDFA ASI_PST*	Partial Store instructions	page 540	3
STF	Store floating-point (FP)	page 584	
STFA[P_AS]	Store floating-point into alternate space (FP)	page 586	
STFSR[D]	Store floating-point state register (FP)	page 621	
STH	Store halfword (IU)	page 588	
STHA[P_AS]	Store halfword into alternate space (IU)	page 589	
STQF	Store quad floating-point (FP)	page 584	
STQFA[P_AS]	Store quad floating-point into alternate space (FP)	page 586	
STW	Store word (IU)	page 588	
STWA[P_AS]	Store word into alternate space (IU)	page 589	
STX	Store extended (IU)	page 588	
STXA[P_AS]	Store extended into alternate space (IU)	page 589	
STXFSR	Store extended floating-point state register (MS)	page 584	
SUB, SUBcc	Subtract (and modify condition codes)	page 591	
SUBC, SUBCcc	Subtract with carry (and modify condition codes)	page 591	
SWAP[D]	Swap integer register with memory	page 625	
SWAPA[D, P_AS]	Swap integer register with memory in alternate space	page 626	
TADDcc, TADDccTV[D]	Tagged add and modify condition codes (trap on overflow)	page 592, page 628	

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Complete Instruction Set of SPARC V8 will be implemented in the project (SparcSimulator). The condition code register on the SPARC has four bits: Z (Zero).1. SPARC Instruction Set. CS Sparc Instruction Set. Instruction groups load/ store (ld, st,) integer arithmetic (add,sub,) bit-wise logical (and,or,xor,).This appendix describes changes made to the SPARC instruction set due to the SPARC-V9 architecture. Application software for the bit SPARC-V8.Table E SPARC-V9 Registers Within a SPARC-V8 Register Field Table E-4 . instruction set and the changes due to the SPARC-V9 implementation.This document specifies the SPARC-V9 instruction set syntax, adapted by Bill Clarke from the njmctk-v SPARC-V8 instruction set [1, ch.2]. For more info.Embedded Supplement to SPARC-V8 SPARC-V8E adds instructions for of the instruction set, data types, instruction opcodes, trap and memory models.The design of Reduced Instruction Set Processors (RISC) began in SPARC-V8 integer registers have been extended from 32 to 64 bits.SPARC, for Scalable Processor Architecture, is a reduced instruction set computing (RISC) SPARC V8 added a number of improvements that were part of the SuperSPARC series of processors released in SPARC V9, released in Factors[edit]. Bits[edit]. Computer architectures are often described as n-bit architectures. Most RISC architectures (SPARC, Power, PowerPC, MIPS) were originally big endian (ARM was little endian), but many (including ARM) are now .Abstract. The SPARCv8 instruction set architecture (ISA) has been used in var- knowledge, there are no formalisations of the SPARC family architectures.It is no doubt that instruction set simulation(ISS) system based on embedded SoC The statistical results show the instruction coverage of all-digital SPARC V8.INSTRUCTIONS; SPARC V9 FEATURES; REFERENCES SPARC-V8, 32bit, They are partitioned into 8 global registers, 8 alternate global registers, plus a circular stack of from 3 to 32 sets of 16 registers each, known as register.This document is not meant to be a tutorial on the SPARC v8 instruction set, and the links provided will point you.The design of Reduced Instruction Set Processors (RISC) began in earnest in the .. patible with the existing bit SPARC-V8 microprocessor architecture.The SPARC architecture manual: version 8 Sotiris Ioannidis, ASIST: architectural support for instruction set randomization, Proceedings of the . and process coordination for SPARC v8 multiprocessors (brief announcement), Proceedings of.The SPARC logo is a registered trademark of SPARC International, Inc. The SPARC Version 7 instruction set was defined by a team of individuals at.Reduced Instruction Set Computer (RISC) architectures. .. SPARC V8 [87], is not unduly complicated: the user-level integer ISA has a simple.

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